LISTING OF CLAIMS

1. (Currently Amended) A data processing system comprising:

a memory for storing operands;

a plurality of general purpose registers wherein each general purpose register holds multiple data elements; and

processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers wherein the at least one or more instructions specifies a number of data elements to be transferred between each of the at least two of the plurality of general purpose registers and the memory, wherein the at least one of the one or more instructions provides a first offset between data elements within a first portion of successive data elements to be stored into the memory or loaded from the memory and a second offset between a first portion and a second portion of the data elements to be stored into the memory or loaded from the memory.

2. (Previously Amended) The data processing system of claim 1 wherein the one or more instructions additionally specifies which of the data elements to load or store in addition to the number of data elements to be transferred.

3. (Original) The data processing system of claim 1 wherein when only a subset of the multiple data elements is transferred between each of the at least two of the plurality of general purpose registers and the memory, any unspecified data elements are filled with a predetermined value.

4. (Original) The data processing system of claim 3 wherein the predetermined value comprises a zero value having all bits equal to zero.

5. (Currently Amended) A method of transferring data elements in a data processing system comprising:

storing operands in a memory;

storing multiple data elements in each of a plurality of general purpose registers; and

executing one or more instructions in the data processing system, at least one of the one or more instructions causing a transfer of a plurality of data elements between the memory and the at least two of the plurality of general purpose registers, wherein the at least one or more instructions specifies a number of data elements to be transferred between each of the at least two of the plurality of general purpose registers and the memory, wherein the at least one of the one or more instructions provides a first offset between data elements within a first portion of successive data elements to be stored into the memory or loaded from the memory and a second offset between a first portion and a second portion of the data elements to be stored into the memory or loaded from the memory.

6. (Previously Amended) The method of claim 5 further comprising:

specifying with each of the one or more instructions which of the data elements to load or store in addition to the number of data elements to be transferred.

7. (Original) The method of claim 5 further comprising:

when only a subset of the multiple data elements is transferred between each of the at least two of the plurality of general purpose registers and the memory, filling any unspecified data elements with a predetermined value.

8. (Currently Amended) A data processing system comprising:

a memory for storing operands;

a plurality of general purpose registers wherein each general purpose register holds multiple data elements; and

processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers wherein the at least one or more instructions specifies which subset of the multiple data elements in each of the at least two of the plurality of general purpose registers are to be transferred, wherein the at least one of the one or more instructions provides a first offset between data elements within a first portion of successive data elements to be stored into the memory or loaded from the memory and a second offset between a first portion and a second portion of the data elements to be stored into the memory or loaded from the memory.

9. (Previously Amended) The data processing system of claim 8 wherein, any unspecified data elements are filled by the processor circuitry with a predetermined value.

10. (Original) The data processing system of claim 9 wherein the predetermined value is a zero value.

11. (Previously Amended) The data processing system of claim 8 wherein the subset of the multiple data elements specified by the at least one or more instructions are contiguously positioned within the at least two of the plurality of general purpose registers.

12. Previously Amended) The data processing system of claim 8 wherein the subset of the multiple data elements specified by the at least one or more instructions are not contiguously positioned within the at least two of the plurality of general purpose registers.

13. (Currently Amended) A method of transferring data elements in a data processing system
comprising:

storing operands in a memory;

holding multiple data elements in each of a plurality of general purpose registers; and

executing one or more instructions, at least one of the one or more instructions causing a transfer of a plurality of data elements between the memory and at least two of the plurality of general purpose registers wherein the at least one or more instructions specifies which subset of the multiple data elements in each of the at least two of the plurality of general purpose registers are to be transferred, wherein the at least one of the one or more instructions provides a first offset between data elements within a first portion of successive data elements to be stored into the memory or loaded from the memory and a second offset between a first portion and a second portion of the data elements to be stored into the memory or loaded from the memory.

14. (Previously Amended) The method of claim 13 further comprising filling any unspecified data elements with a predetermined value.

15. (Currently Amended) A data processing system comprising:

a memory for storing operands;

a plurality of general purpose registers wherein each general purpose register holds multiple data elements; and

processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring a plurality of data elements between the memory and the at least two of the plurality of general purpose registers wherein the at least one or more

instructions specifies both a number of data elements to be transferred between each of the at least two of the plurality of general purpose registers and the memory and further specifies a total number of data elements to be transferred, wherein the at least one of the one or more instructions provides a first offset between data elements within a first portion of successive data elements to be stored into the memory or loaded from the memory and a second offset between a first portion and a second portion of the data elements to be stored into the memory or loaded from the memory.

16. (Original) The data processing system of claim 15 wherein when a total number of data elements to be transferred is greater than a number of data elements to be transferred to each of the at least two of the plurality of general purpose registers, data elements are transferred to a predetermined one of the plurality of general purpose registers.

17. (Original) The data processing system of claim 15 wherein when a total number of data elements to be transferred is less than a number of data elements to be transferred to each of the at least two of the plurality of general purpose registers, any remaining specified data elements of the plurality of general purpose registers are filled with a predetermined value.

18. (Original) The data processing system of claim 17 wherein the predetermined value is a zero value.

19. (Original) The data processing system of claim 15 wherein the one or more instructions specifies by using a field in the instruction to identify the number of data elements to be transferred between each of the at least two of the plurality of general purpose registers and the memory and to identify the total number of data elements to be transferred.

20. (Original) The data processing system of claim 15 wherein the one or more instructions specifies by identifying a register within the data processing system that contains information to identify the number of data elements to be transferred between each of the at least two of the plurality of general purpose registers and the memory and to identify the total number of data elements to be transferred.

21. (Original) The data processing system of claim 15 wherein the data elements are positioned in contiguous storage locations in the memory.

22. (Original) The data processing system of claim 15 wherein the data elements are positioned in non-contiguous storage locations in the memory.

23. (Previously Presented) The data processing system of claim 1, wherein the number of data elements specified by the at least one or more instructions specifies only a subset of the multiple data elements in each of the at least two general purpose registers to be transferred.